

**ELE339, Electronics I Laboratory**  
**LAB 9 - MOS Transistor Modeling**

**Introduction**

**Objective:**

In this lab, we investigate an n-channel enhancement mode MOS transistor. This device, and its complement, the p-channel enhancement mode MOS transistor, represent the work horses of today's semiconductor industry. Thanks to the comparatively simple geometry, the channel length of a state-of-the-art MOS transistor can be as short as 40nm. These ultra short channel length devices support switching frequencies in the GHz range.

**Device Characteristics**

Figure 1 shows the cross section, the top view and the symbol used for an n-channel MOS transistor.

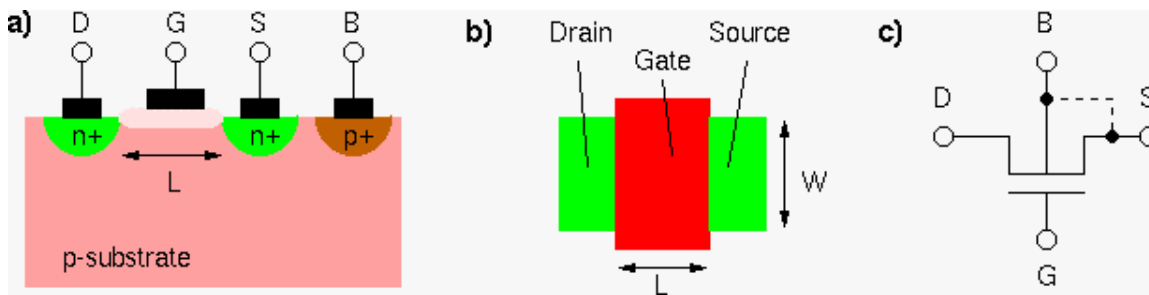


Figure1: a) Cross section, b) top view and c) symbol on an enhancement mode n-channel MOS transistor.

If we apply a minimum positive voltage (*threshold voltage*) between the gate and the body B of the transistor, we create a thin sheet of electrons at the very surface of the semiconductor underneath the gate. This *inversion layer* forms a *resistive* connection between the drain and the source contacts and thus acts similar to a resistor. As long as the drain voltage remains small, we can approximate the drain-source current to drain-source voltage characteristic by the following equation

$$I_{D_{triode}} = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2] \quad (1)$$

where W and L are the channel width and length, respectively,  $\mu$  the carrier mobility and  $C_{ox} = \epsilon_{ox}/t_{ox}$  the oxide capacitance. This operating mode of the device is referred to as *ohmic* or *triode* operation. If we continue to increase the drain potential, we progressively reduce the inversion layer on the drain side until we end up with a small region, which features no mobile charge carriers at all (*depletion region*). If the drain potential is further increased beyond this *saturation voltage*, the drain-source current remains approximately constant (*saturated*). The corresponding device equation for this region is

$$I_{D_{sat}} = \frac{1}{2} \mu C_{ox} \frac{W}{L} [V_{GS} - V_{th}]^2 \quad (2)$$

The minimum drain-source voltage for *saturation* is

$$V_{D_{sat}} = V_{GS} - V_{th} \quad (3)$$

## Pre-Lab

### Tasks:

1. Set up a circuit that allows you to simulate, using Pspice, the input characteristics, i.e.,  $I_D$  vs.  $V_{GS}$ , of the 2N7000 MOS transistor. To do so, keep the drain of the device at a constant potential while the source remains grounded. Note: the source and body of this device are shorted.
2. From the plot of the input characteristics find a way to graphically deduce the threshold voltage of your transistor and the value of the product  $K=\mu C_{ox} W/L=k_p W/L$ . Hint, if the drain voltage is very small, the I-V characteristic becomes linear.
3. Consider the circuit in figure 2 and find an expression for the current  $I_{ref}$ . Hint: Transistor M1 is operated in the saturation region.
4. Find a numerical value for  $I_{ref}$  if  $V_{DD}=10V$  and  $R_{ref}=10k\Omega$ . To do so, use the values for  $K$  and  $V_{th}$  you deduced from your plots in task 2. How is the current through M2 related to  $I_{ref}$ ?
5. Use Pspice to plot the current  $I_{d2}$  of M2 in the circuit of Fig. 2 as a function of  $V_d$  as  $V_d$  is in the range of 0 – 10V (Set  $V_{DD}=10V$  and select  $R_{ref}=10k\Omega$ ).
6. From the output characteristic of M2 deduce an approximate value for the output resistance  $r_o$  of M2.
7. Repeat task 5 with  $R_{ref}=4.7k\Omega$ . By considering both output characteristics (of tasks 5 and 7) find an approximate value for the transconductance  $g_m$  of the MOS device?

## Experimental

8. Set up a circuit that allows you to measure the input characteristics of task 1 and compare the measured to the simulated results.
9. Build the circuit depicted in figure 2 on your Protoboard and record the drain current  $I_{d2}$  of M2 while you raise  $V_d$  from 0 – 10V in steps of 0.5V (Set  $V_{DD}=10V$  and select  $R_{ref}=10k\Omega$ ). Compare your results to the simulated ones in task 5.

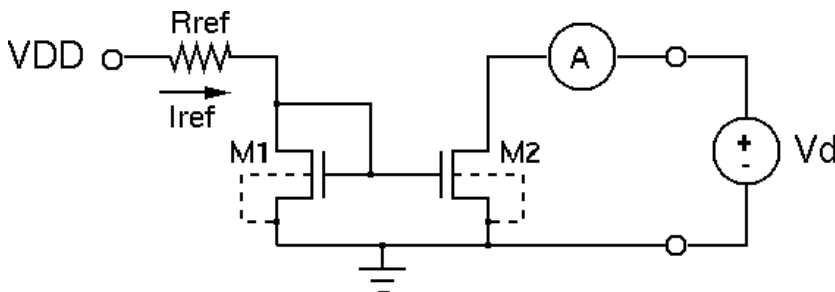


Figure 2: MOS transistor with current source biasing.